



MRC/CET



a step of forming an insulating film between electrodes at at least a side wall of the first electrode;

a step of forming a second layer conductive film constituting a second electrode on the surface of the semiconductor substrate formed with the first electrode and the insulating film between electrodes; and

a step of flattening the second layer conductive film.

15. (Withdrawn) The method of producing a solid image pick-up element according to Claim 14,

wherein the step of flattening the second layer conductive film includes:

a step of coating a resist at an upper layer of the second layer conductive film by a spin coating method; and

a step of flattening the second layer conductive film by a resist etch back method.

16. (Withdrawn) The method of producing a solid image pick-up element according to Claim 15,

wherein the step of forming the pattern of the first layer conductive film comprises:

a step of forming the pattern including a dummy pattern such that a surface level of the resist does not become to be equal to or smaller than a predetermined value on the semiconductor substrate.

17. (Withdrawn) The method of producing a solid image pick-up element according to Claim 14,

wherein the step of flattening the second layer conductive film includes:

a step of flattening the second layer conductive film by a CMP (chemical mechanical polishing) method.

18. (Withdrawn) The method of producing a solid image pick-up element according to Claim 17,

a step of forming the pattern including a dummy pattern such that a surface level of the second layer conductive film does not become equal to or smaller than a predetermined value on the semiconductor substrate.

wherein the flattening step is a step for executing resist etch back by constituting a stopper by the stopper layer.

wherein the flattening step is a step of executing CMP by constituting a stopper by the stopper layer.

wherein the gate oxide film is formed between the wiring layer for the peripheral circuit portion and the semiconductor substrate.